LISTING OF CLAIMS:

Claims 1-3 (Canceled)

4. (Original) A nonvolatile ferroelectric memory control device comprising:

a page address buffer for latching a page address having a block page address region and a column page address region in response to a chip enable signal, and for decoding the latched page address;

a row address latch unit for latching a row address in response to the chip enable signal, and for outputting the latched row address;

an address transition detector for detecting transition of the latched row address, and for outputting an address transition detecting signal;

a reset signal transition detector for detecting transition of a reset signal in response to the chip enable signal, and for outputting a reset transition detecting signal;

a write enable signal transition detector for detecting transition of a write enable signal in response to the chip enable signal, and for outputting a write enable transition detecting signal;

a synthesizer for outputting a transition synthesizing signal in response to the address transition detecting signal, the reset transition detecting signal and the write enable transition detecting signal; and

a chip control signal generator for selectively generating a control signal to control a chip operation in response to the transition synthesizing signal.

5. (Original) The device according to claim 4, wherein the row address is arranged in more significant bit region, a column page address of the page address is arranged in less significant bit region, and a block page address of the page address is arranged between the row address region and the column page address region.

6. (Original) The device according to claim 4, wherein the page address buffer comprises:

a page address latch unit for latching a page address in response to the chip enable signal, and for outputting the latched page address; and

a page decoder for decoding the latched page address.

7. (Original) The device according to claim 6, wherein the page address latch unit comprises:

a page address controller for latching the page address in response to the chip enable signal, and for selectively outputting the latched page address; and

a first output means for delaying an output signal from the page address controller, and for outputting the latched page address.

8. (Original) The device according to claim 4, wherein the row address latch unit comprises:

a row address controller for latching the row address in response to the chip enable signal, and for selectively outputting the latched row address;

a latch controller for latching an output signal from the row address controller in response to a latch control signal, and for selectively outputting the latched output signal; and

a second output means for delaying an output signal from the latch controller, and for outputting the latched row address.

9. (Original) The device according to claim 4, wherein the reset signal transition detector comprises:

a reset signal detector for latching a high voltage level while the chip enable signal is disabled before the reset signal transits to a low level in an initial stage of the memory cell operation; and

a pulse generator for generating the reset transition detecting signal having a pulse width for a predetermined delay time depending on the high voltage level.

10. (Original) The device according to claim 9, wherein the reset signal detector comprises:

an input controller for detecting transition of the reset signal and the chip enable signal;

a driver, driven in response to an output signal from the input controller, for selectively outputting a power voltage or a ground voltage; and

a latch unit for latching an output signal from the driver for a predetermined time.

11. (Original) The device according to claim 9, wherein the pulse generator comprises:

a delay unit for delaying an output signal from the reset signal detector for a predetermined time; and

a logic unit for performing a logic operation on output signals from the reset signal detector and the delay unit, and generating the reset transition detecting signal.

Claims 12-28 (Canceled).